REMARKS

Claims 17 through 27 were rejected and have been canceled.

New claims 28 through 39 have been added.

The applicant respectfully requests reconsideration in light of the amendments and the following comments.

35 U.S.C. 103 Rejection of Claims 17-27

Each of claims 17 through 27 were rejected under 35 U.S.C. 103(b) as being unpatentable over various combinations of four references:

1. D.A. Klein, U.S. Patent 5,666,522, issued 9 September 1997 (hereinafter "Klein"),
2. Kiuchi et al., U.S. Patent 4,958,276, issued 18 September 1990 (hereinafter "Kiuchi"),
3. M. Touriguian et al., U.S. Patent 5,832,257, issued 3 November 1998 (hereinafter "Touriguian"), and
4. K. Takeda, U.S. Patent 5,319,771, issued 7 June 1994 (hereinafter "Takeda").

Claims 17 through 27 were canceled, without prejudice, and the applicant respectfully retains the right to re-introduce those claims in this or a later application.

New claims 28 through 39 have been added, and the applicant respectfully submits that these claims are allowable.

New claim 28 recites:

> **28.** An apparatus comprising:
>
> circuitry for receiving a source clock signal from an external device and for *receiving data from said external device at a rate equal to the frequency of said source clock signal*; and
>
> a function clock generator that *generates a function clock signal from said source clock signal, wherein said function clock signal alternates between having the same frequency as said source clock signal and twice the frequency as said source clock signal.*
>
> (*emphasis supplied*)

Nowhere do the references teach or suggest, alone or in combination, what claim 28 recites – namely (i) that the apparatus receives a source clock signal from an external device and receives data from that device at the frequency of the source clock signal, (ii) a functional clock generator that generates a function clock signal from the source clock

signal, or (iii) that the function clock signal alternates between having the same frequency as the source clock signal and having twice the frequency as the source clock signal.

This is advantageous for two reasons.

First, there is always zero phase error between the source clock signal and the function clock signal, and, therefore, the apparatus can always maintain phase synchronization with the external device with which it is communicating.

Second, the fact that there is always zero phase error between the source clock signal and the function clock signal means that the function clock signal can alternate between the source clock frequency and twice the source clock frequency on a period-by-period basis. This enables the apparatus to be highly efficient because there is no transition or re-adjustment interval when the function clock signal changes frequency (*i.e.*, there is no risk of metainstability).

For these reasons, the applicant respectfully submits that claim 28 is allowable.

Because claims 29 through 33 depend on claim 28, the applicant respectfully submits that they too are allowable.

New independent claim 34 recites:

> **34.** An apparatus comprising:
>
> circuitry for receiving a source clock signal from an external device and for *transmitting data to said external device at a rate equal to the frequency of said source clock signal*;
>
> a function clock generator that *generates a function clock signal from said source clock signal, wherein said function clock signal alternates between having the same frequency as said source clock signal and twice the frequency as said source clock signal.*
>
> (emphasis supplied)

Claim 34 is identical to claim 28 except that it recites the transmission of data to the external device instead of the reception of data from the external device, as is recited in claim 28.

For the same reasons as those given with respect to claim 28, nowhere do the references teach or suggest, alone or in combination, what claim 28 recites – namely (i) that the apparatus receives a source clock signal from an external device and transmits data to that device at the frequency of the source clock signal, (ii) a functional clock generator that generates a function clock signal from the source clock signal, or (iii) that the function clock signal alternates between having the same frequency as the source clock signal and having twice the frequency as the source clock signal.

For these reasons, the applicant respectfully submits that claim 34 is allowable.

Because claims 35 through 39 depend on claim 24, the applicant respectfully submits that they too are allowable.

Request for Reconsideration Pursuant to 37 C.F.R. 1.111

Having responded to each and every ground for objection and rejection in the Office action mailed 29 March 2004, applicants request reconsideration of the instant application pursuant to 37 CFR 1.111 and request that the Examiner allow all of the pending claims and pass the application to issue.

Should there remain unresolved issues the applicant respectfully requests that Examiner telephone the applicants' attorney at 732-578-0103 x11 so that those issues can be resolved as quickly as possible.

Respectfully,
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